Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1-5 (cancelled)

Claim 6 (currently amended): A phase locked loop circuit with dual gate dielectric thicknesses, comprising:

an oscillator to output a reference clock signal;

a reference frequency divider to receive and divide the reference clock signal, and output a reference signal;

a comparison frequency divider to receive a control voltage signal and output a comparison signal;

a phase comparator to receive the reference signal and the comparison signal, wherein said phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal;

a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal;

a low-pass filter to receive the charge pump signal and output a low pass filter signal; and

a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal,

wherein said oscillator, said reference frequency divider, said comparison frequency divider, said phase comparator, said charge pump, and said voltage controlled oscillator comprise devices having thin gate oxide layers;

wherein said low-pass filter comprises a capacitor formed by

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide layer formed over said P-type region;

a P^+ gate electrode formed over said thick oxide layer and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent ~~the~~ said gate electrode and coupled to a second voltage supply line; and

wherein said thick oxide layer of said capacitor reduces leakage current such that a gate-to-substrate voltage of said capacitor is maintained, thereby maintaining a stable control voltage for the phase locked loop circuit.

Claim 7 (currently amended): The circuit of claim 6, wherein [[a]] the gate-to-substrate voltage of said capacitor is maintained at less than zero volts.

Claim 8 (original): The circuit of claim 6, wherein said P^+ gate comprises polysilicon.

Claim 9 (original): The circuit of claim 6, wherein said N-type substrate comprises a deep NWELL.

Claim 10 (currently amended): The circuit of claim 6, wherein said thick oxide layer is between about 20 and 100 Å thick.

Claim 11 (currently amended): In a low-pass filter for a phase locked loop (PLL) circuit with dual gate dielectric thicknesses, wherein the PLL circuit additionally includes an oscillator, a reference frequency divider, a comparison frequency divider, a phase comparator, a charge pump, and a voltage controlled oscillator each comprising devices having thin gate oxide layers, a capacitor comprising:

an N-type substrate;

a P-type region within said N-type substrate;

a thick oxide layer formed over said P-type region;

a P^+ gate electrode formed over said thick oxide layer and coupled to a first voltage supply line; and

P^+ pick-up terminals within said P-type region adjacent ~~the~~ said gate electrode and coupled to a second voltage supply line,

wherein said thick oxide layer of the capacitor reduces leakage current whereby a gate-to-substrate voltage of the capacitor is maintained at less than zero volts to maintain a stable control voltage for the PLL circuit.

Claim 12 (cancelled)

Claim 13 (original): The capacitor of claim 11, wherein said P^+ gate electrode comprises polysilicon.

Claim 14 (original): The capacitor of claim 11, wherein said N-type substrate comprises a deep NWELL.

Claim 15 (currently amended): The capacitor of claim 11, wherein said thick oxide layer is between about 20 and 100 Å thick.

Claim 16-24 (cancelled)

Claim 25 (new): A phase locked loop circuit with dual gate dielectric thicknesses, comprising:

an oscillator to output a reference clock signal;

a reference frequency divider to receive and divide the reference clock signal, and output a reference signal;

a comparison frequency divider to receive a control voltage signal and output a comparison signal;

a phase comparator to receive the reference signal and the comparison signal, wherein said phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal;

a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal;

a low-pass filter to receive the charge pump signal and output a low pass filter signal; and

a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal,

wherein said oscillator, said reference frequency divider, said comparison frequency divider, said phase comparator, said charge pump, and said voltage controlled oscillator comprise devices having thin gate oxide layers;

wherein said low-pass filter includes a capacitor that comprises at least one device having a thick gate oxide layer; and

wherein said thick gate oxide layer of said capacitor reduces leakage current such that a gate-to-substrate voltage of said capacitor is maintained, thereby maintaining a stable control voltage for the phase locked loop circuit.